

C2 versus C3

- C2 crossbar distributed across each memory board; 72 GA required for full system. C3 crossbar is a separate physically assembly requiring 38 GA.
- C2 memory board is 32 bits wide with eight banks. A C3 board is 64 bits wide with 32 banks.
- C2 memory boards have one 7K ECC GA per bank. C3 boards use a total of 4 bank control GA, 1 read EDC GA, and 32 write EDC GA.
- C2 memory boards can accomodate 256K, 1M, 4M RAMs with up to four rows per bank. C3 boards are designed for 1M and 4M RAMs with no row expansion.

Table -1: Approximate Cycle and Access Times, 80ns RAMs

| Operation | Cycle Time | Access Time (at crossbar) | Access Time (at processor) |
|------------------------------|------------|------------------------------|-------------------------------|
| NOP | 15 | -- | -- |
| Read | 15 | 13 | 19 |
| Read w/ECC error | 15 | 13 | 19 |
| Full Write | 15 | -- | -- |
| Partial Write | 21 | -- | -- |
| Partial Write w/ECC error | 42 | -- | -- |
| TAM | 21 | 13 | 19 |
| TAM w/ECC error | 42 | 13 | 19 |

MIM V2.1 LAYOUT

HEX LEVEL TRANSLATORS
JULY 20, 1988

1.95 INCHES HIGH

CONNECTOR

| IO | PINS |
|---------|-------|
| RAS | 1 |
| CAS | 1 |
| WE | 1 |
| ADDRESS | 11 |
| DI | 36 |
| DO | 39 |
| CONTROL | 9 |
| STATUS | 3 |
| ERR LOG | 3 |
| | <hr/> |
| | 104 |
| POWER | 21 |

-> 128 PIN CONNECTOR

TERMINATORS:

43 X 1 KOHM (T-E) --> 3 NETWORK PACKAGES
60 X 100 OHM (E-T) --> 4 NETWORK PACKAGES
60 X 22 OHM (E-T) --> 4 NETWORK PACKAGES

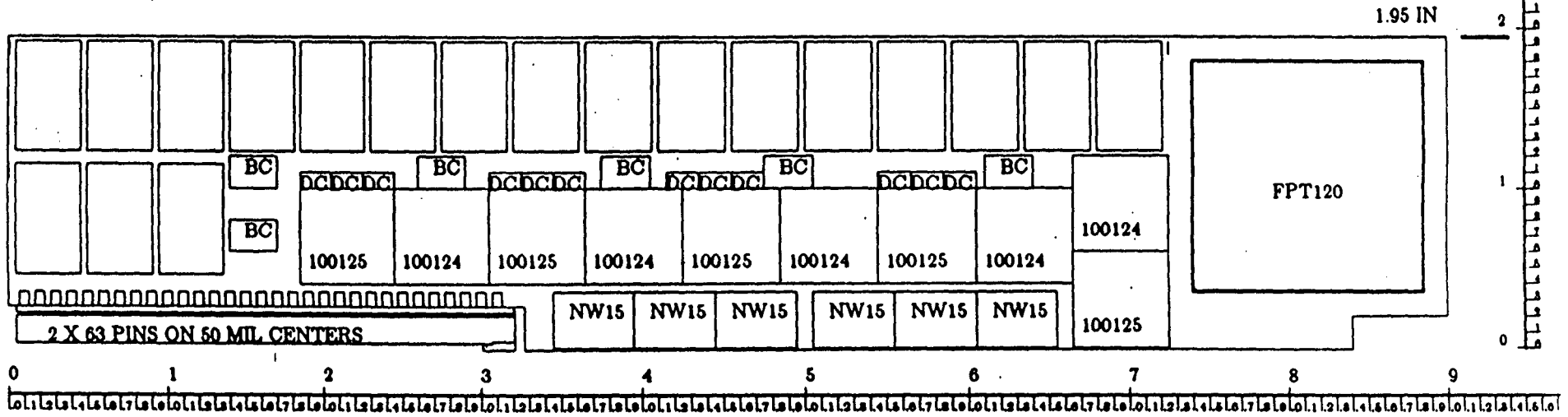
11 NETWORK PACKAGES

CAPACITORS:

10 X 33UF BC (RAM BC)
27 X .1UF BC (3 PER 8483)
39 X .33UF DC (UNDER EACH RAM; NOT SHOWN)

XLATORS:

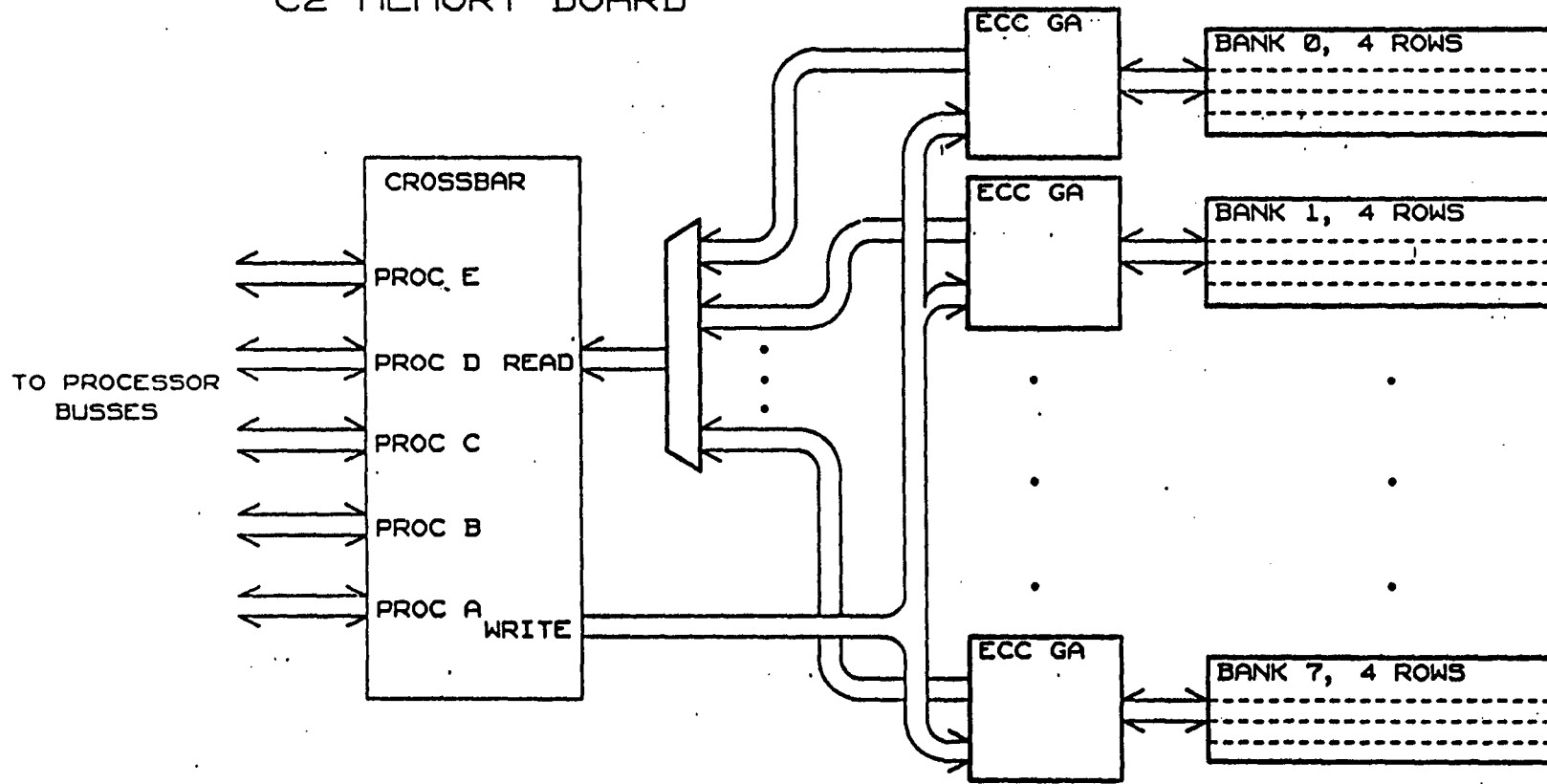
61 INPUT --> 11 X 100124
43 OUTPUT --> 8 X 100125



ONE SIDE

JON GELSE

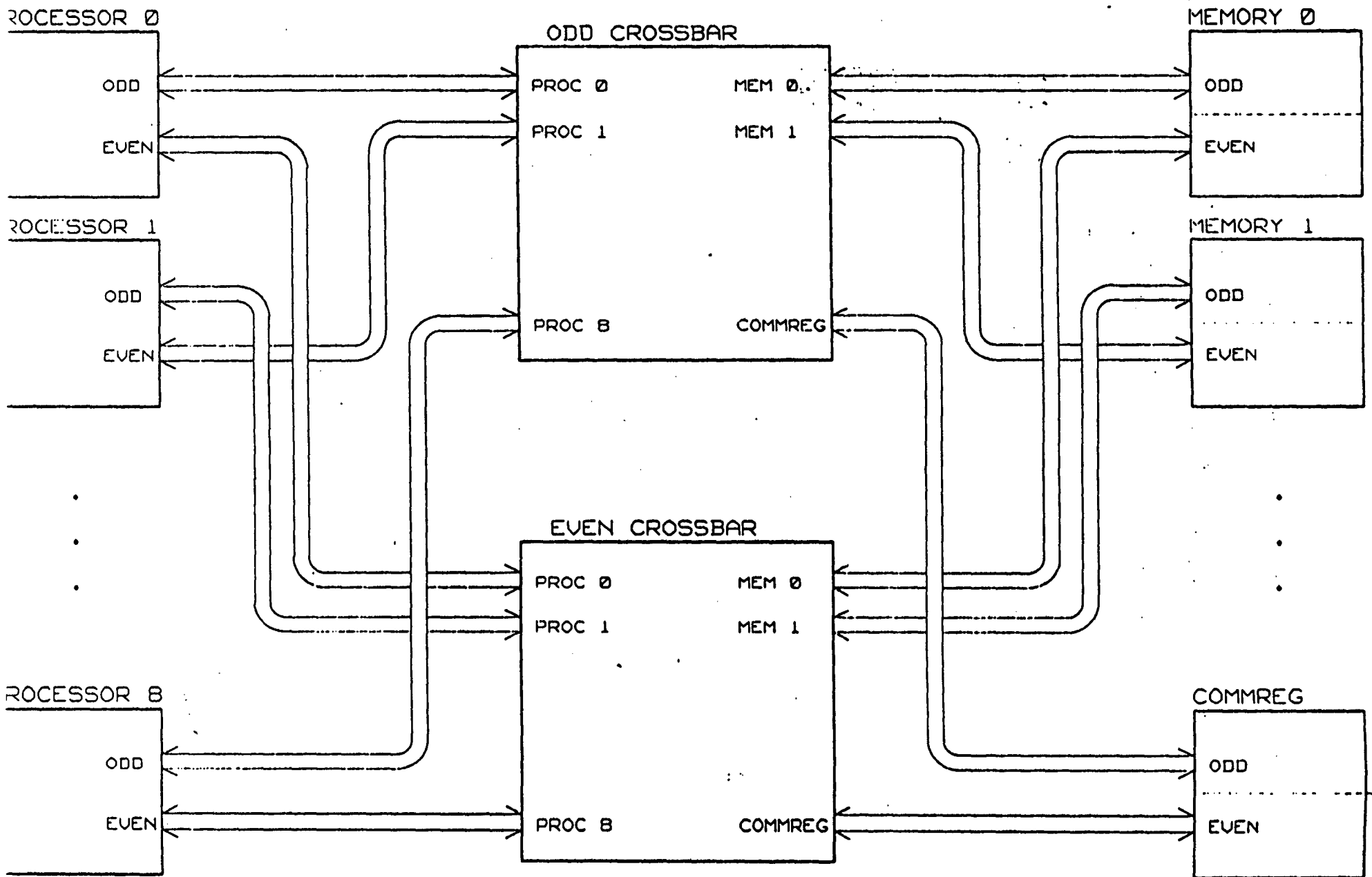
C2 MEMORY BOARD



CONVEX

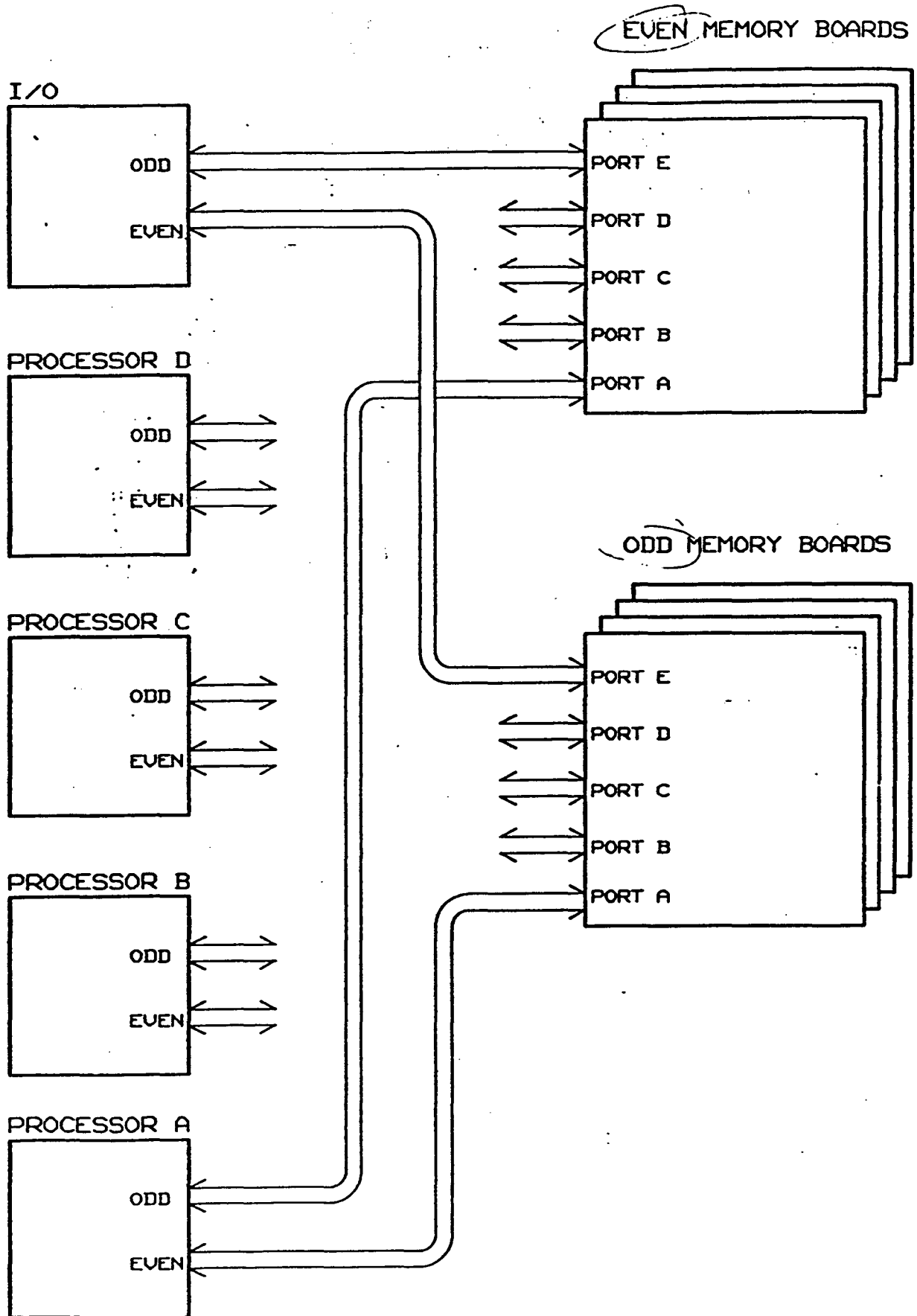
Figure

C3 MEMORY SYSTEM

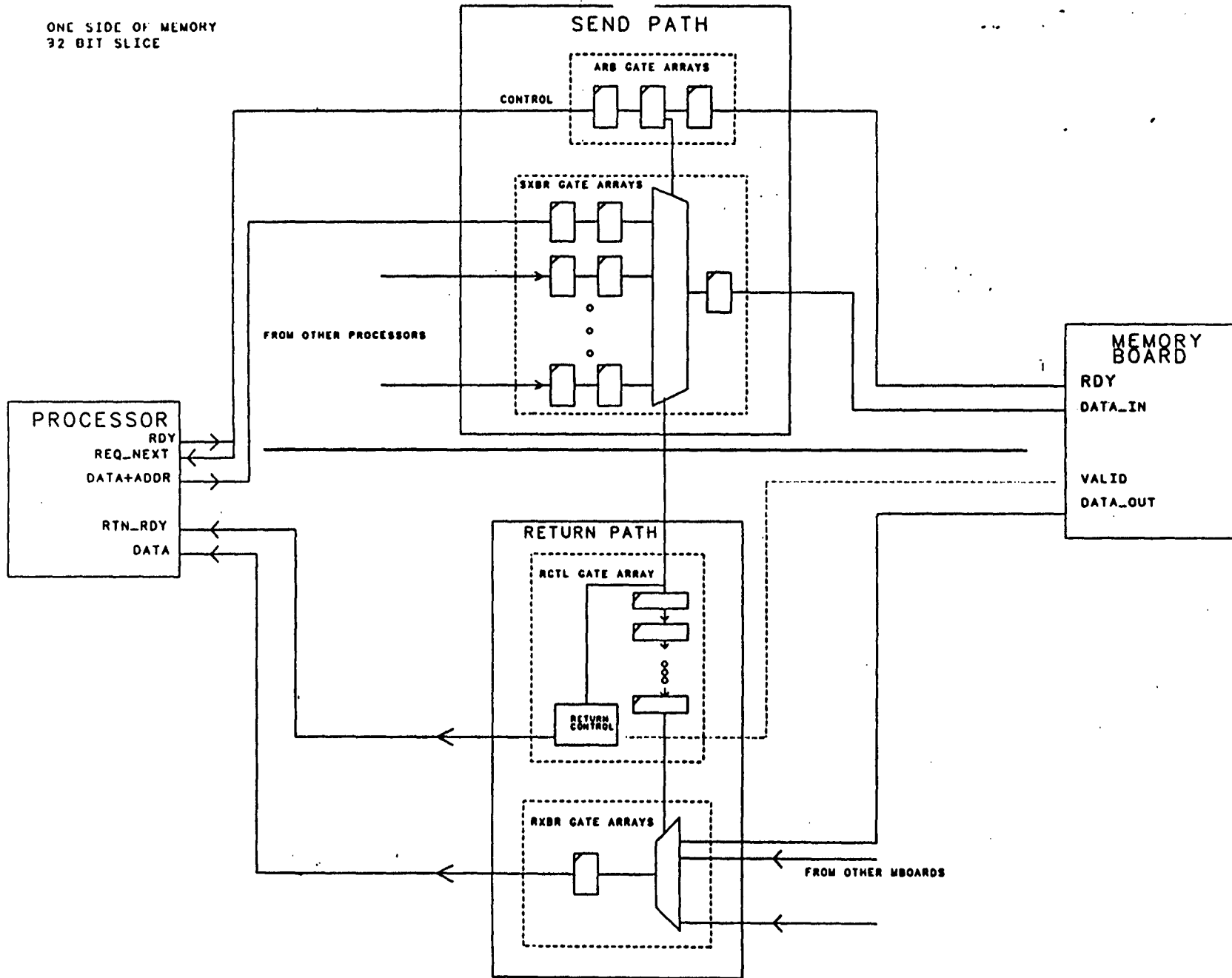


CONVEX

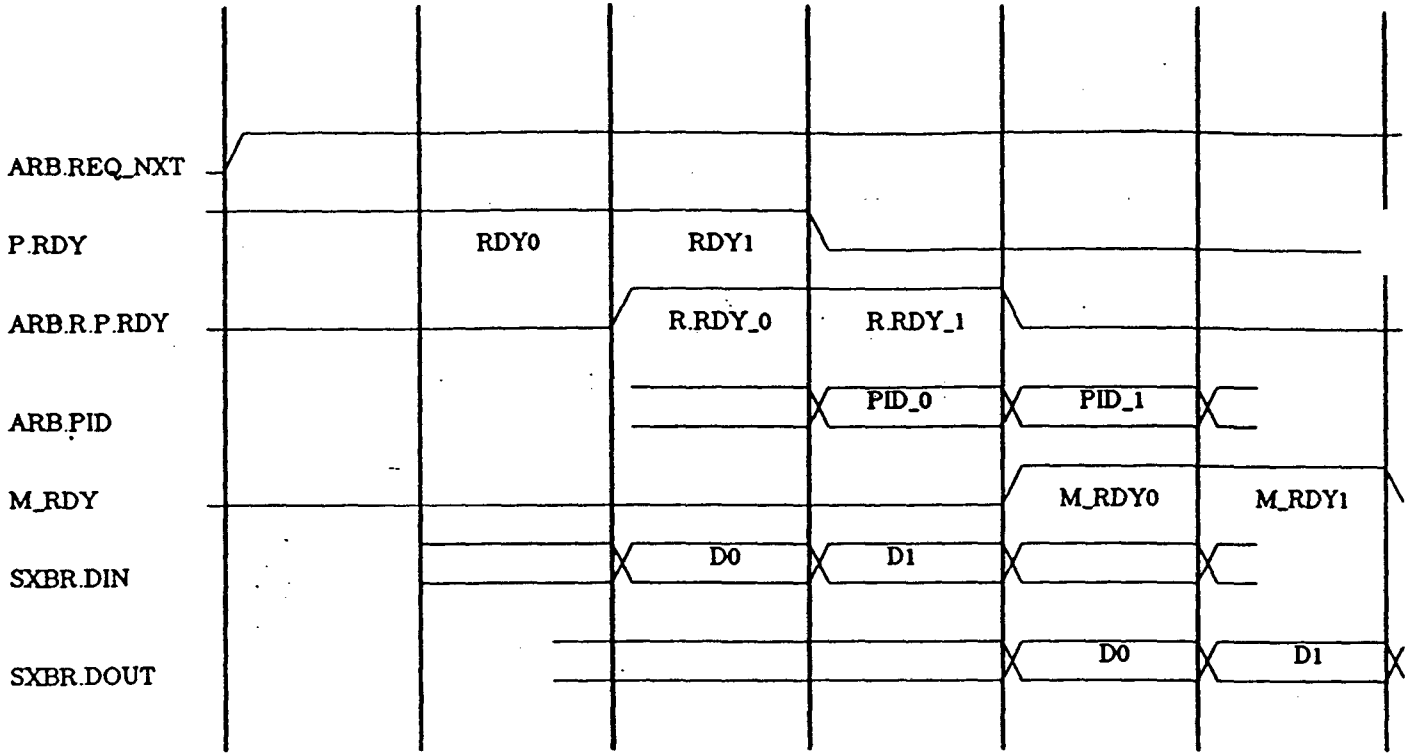
C2 MEMORY SYSTEM



ONE SIDE OF MEMORY
32 BIT SLICE



11



BLOCKED REQUEST

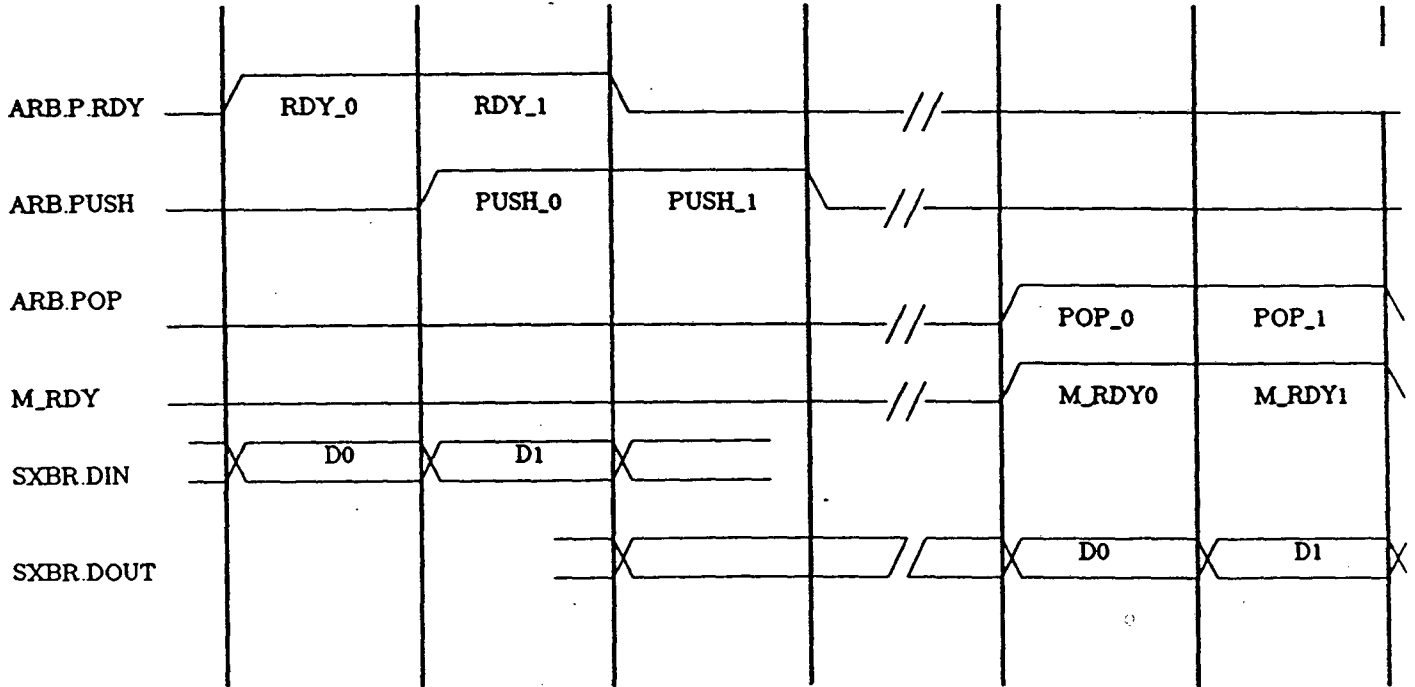
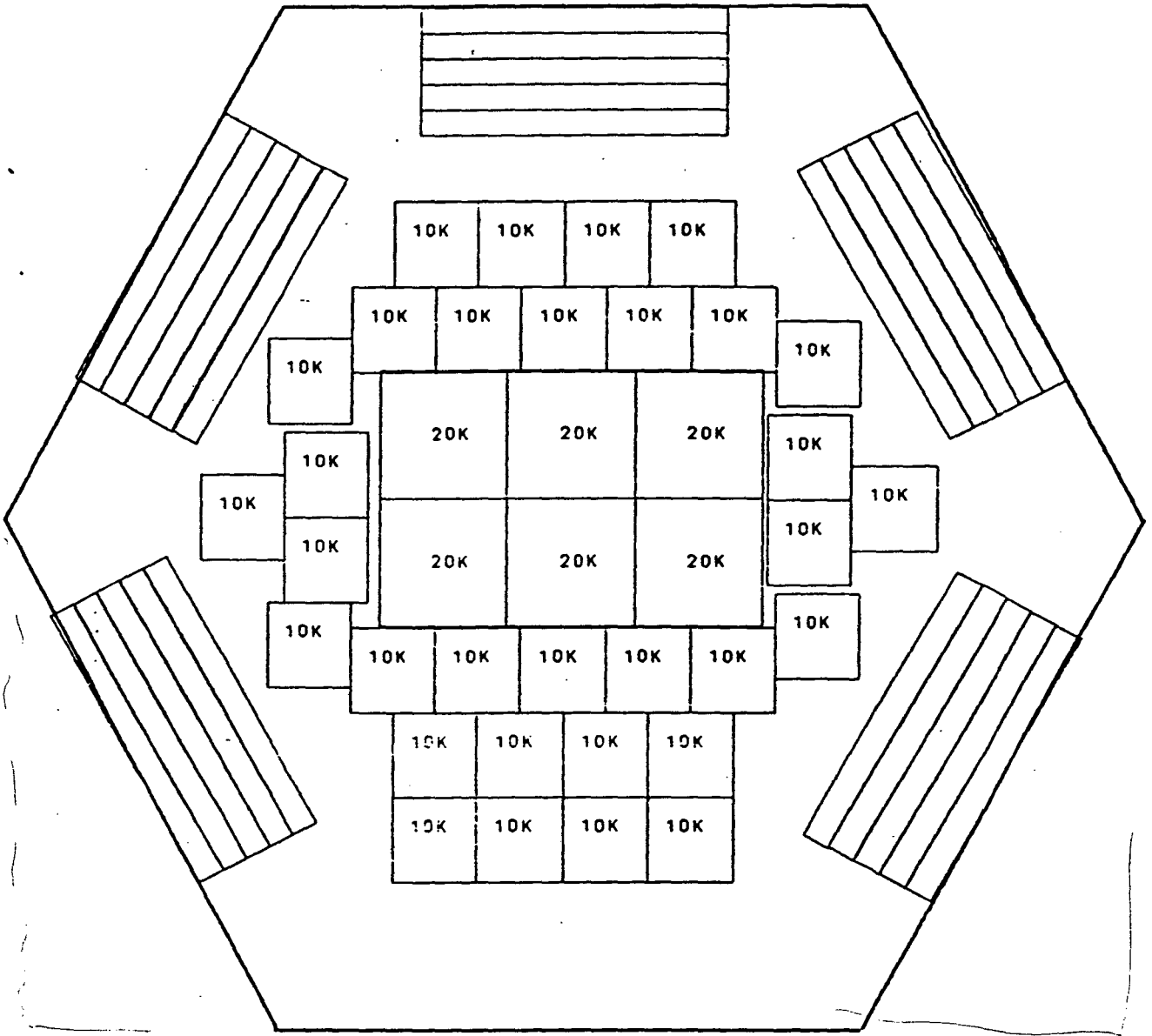


FIGURE 13
SEND CROSSBAR TIMING

24 IN



13.86 IN

27.72 IN



CONVEX

TITLE: BOARD
 DRAWING: 000-000000-000a n
 REVISED: Thu Sep 22 16:58:07 1986

ABBR: X9AR BOARD
 ENGR: GELSEY
 PAGE: 1

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Crossbar Gate Arrays

Four Gate Array Types Are Used on the Crossbar

- 4 ARB 20K's
 - 238 out of 256 I/O, Cellcount at 85%
- 22 SXBR 10K's
 - 186 out of 192 I/O, Cellcount at 89%
- 2 RCTL 20K's
 - 116 out of 256 I/O, Cellcount at 51%
- 10 RXBR 10K's
 - 169 out of 192 I/O, Cellcount at 58%

6 20K's Total

32 10K's Total

38 Total Gate Arrays on Crossbar
to Cover Both Even and Odd Sides

Crossbar Gate Array Issues

ARB Issues

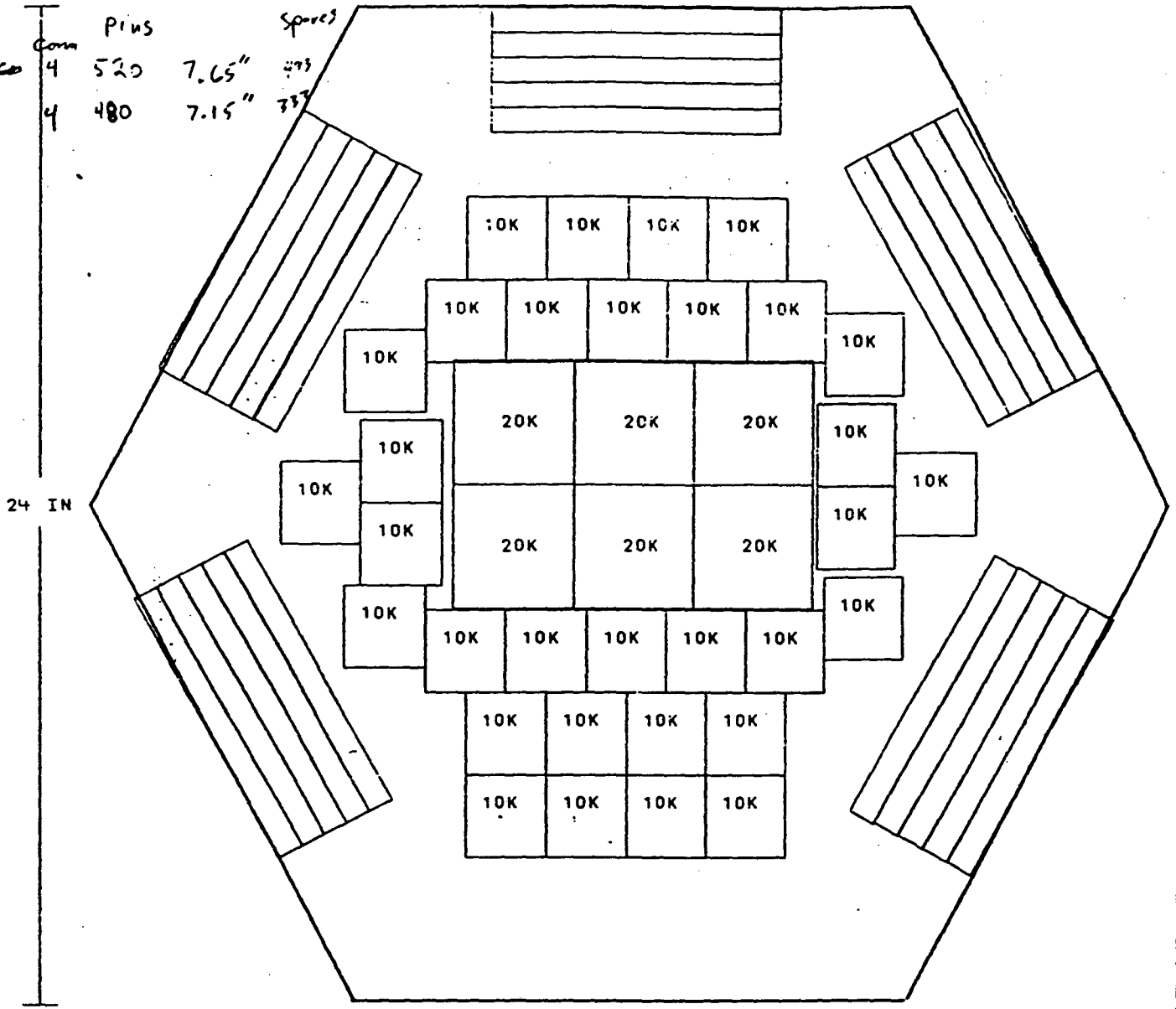
- The ARB gate array is 85% percent full as currently envisioned and may overflow.
 - The current plan is to use two ARB's per side. By splitting the ARB function into three gate arrays the cellcount can be reduced by about 15% per array.
- A timing path within the ARB is fairly tight and might not be made.
 - Latency through the crossbar might extend by one extra cycle.

SXBR Issue

- The SXBR gate array is 89% full as currently envisioned and may overflow.
 - By reducing the data slice an SXBR handles to 6 bits from 7, the cellcount drops by about 14% per array. However, it will be necessary to use at least one extra SXBR gate array per side; since this scheme leaves no free data pins it might require a total of two more 10K's per side.

.1 \Rightarrow 2.5 grids per "

Conn Pins Spares
 4 520 7.65" 475
 4 480 7.15" 337



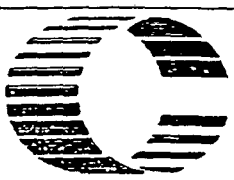
24 IN

13.86 IN

27.72 IN

Assumes 2" x 2" for 10K
 3" x 3" for 20K

- + 4 10K arrays out/1
- + 2 20Ks Arb out/1
- + 250 termination pts
- + 20 Eclipse pts
- + 2 10K gate arrays for clocks
- + 750 ? Eclipse pts for Comm



CONVEX

| | |
|--|------------------|
| TITLE: BOARD | ABBR: XBAR BOARD |
| DRAWING: 000-000000-000c n - | ENGP: GELSEY |
| REVISED: Thu Sep 22 16:58:07 1988 | PAGE: 1 |
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| --> 126 PIN CONNECTOR | |

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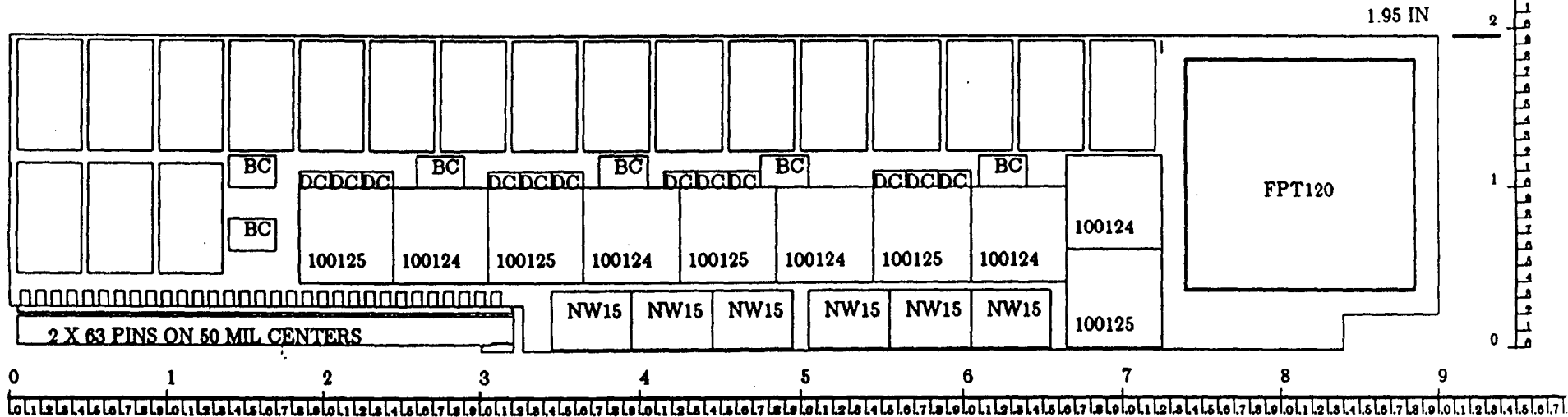
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ONE SIDE

JON GELSEY

CROSSBAR

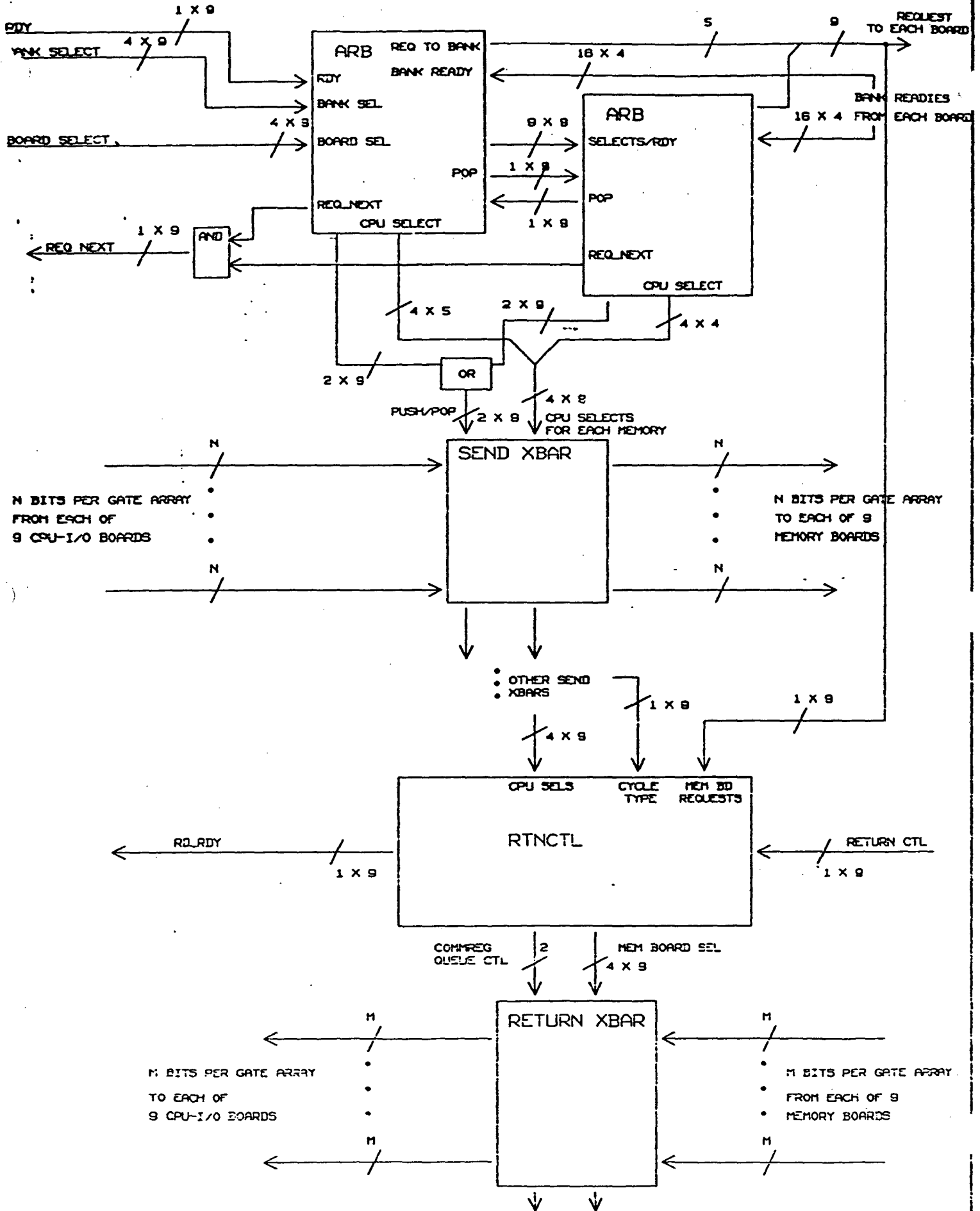
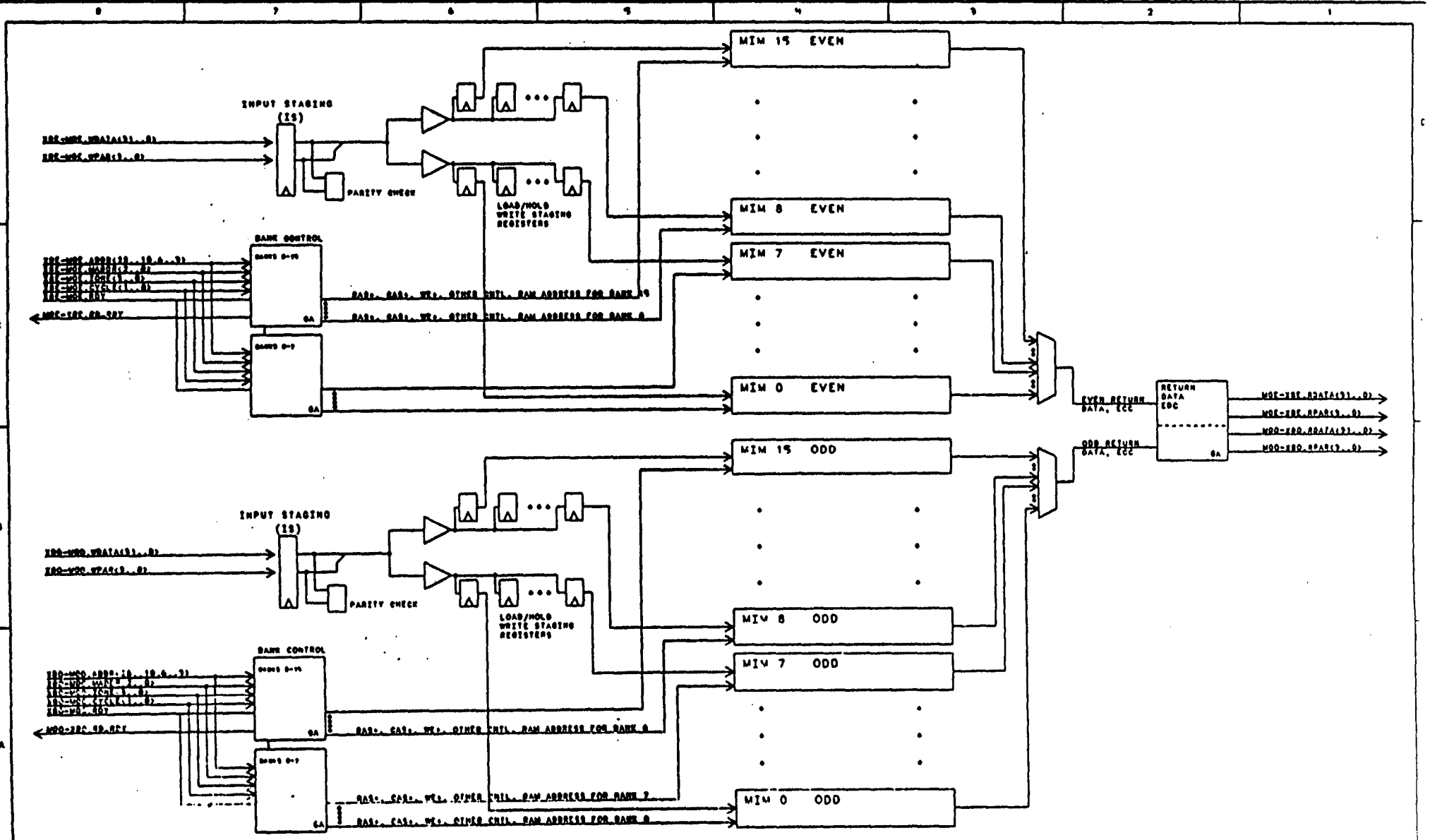


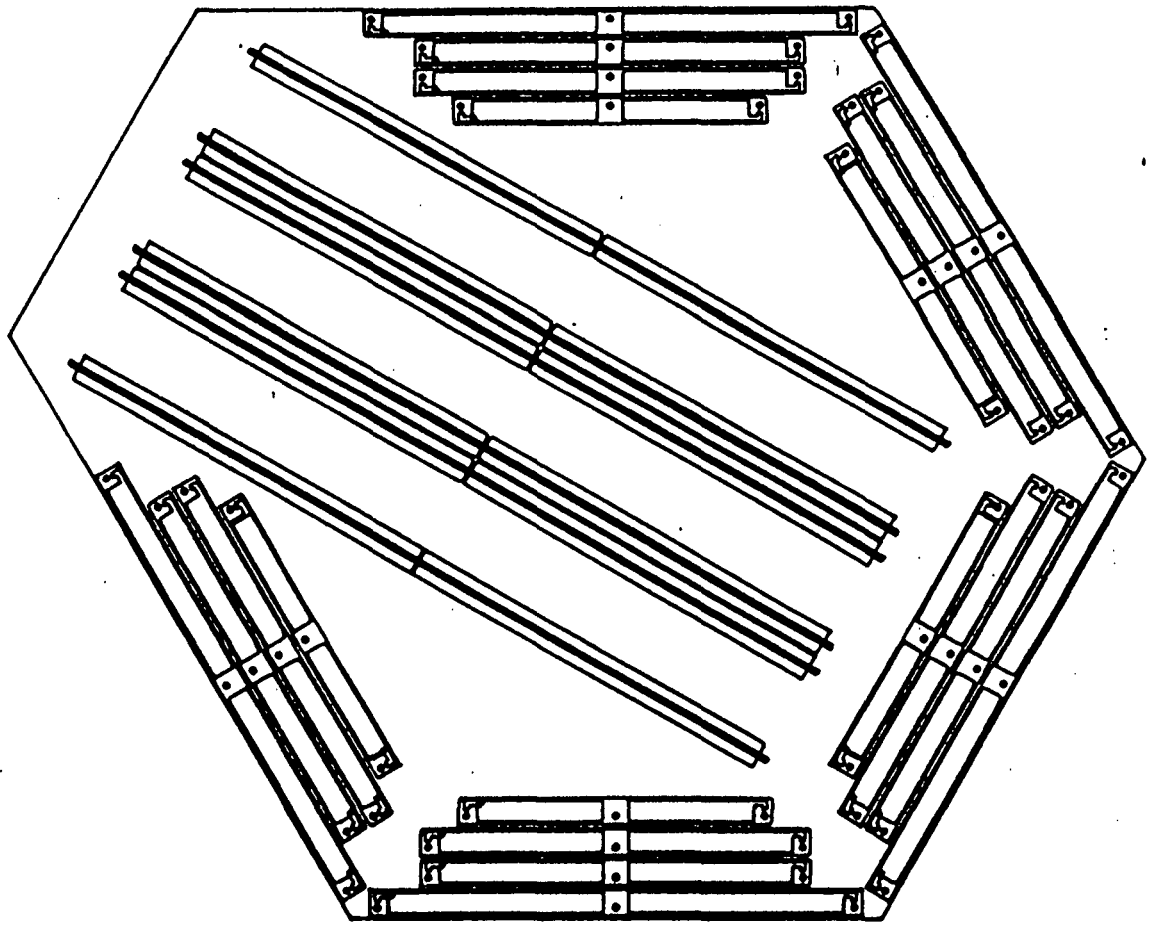
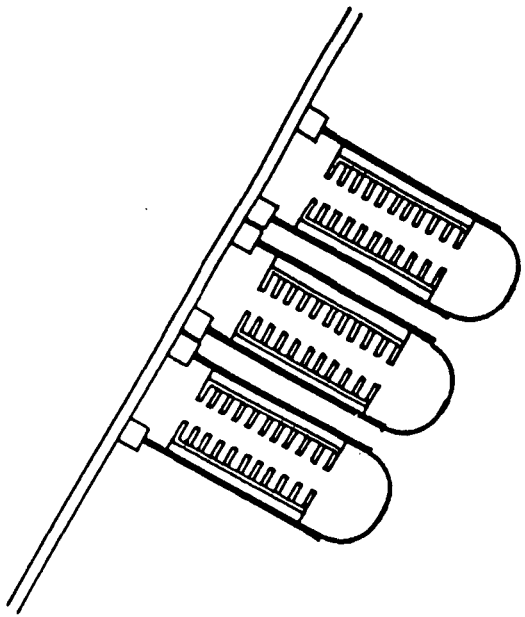
Figure 1-1



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| | | |
|----------------------------|--------------|------------------|
| TITLE: MIM OVERVIEW | | APPR: MMD |
| DRAWING: 000-000000-0000 A | | ENGR: GUYTROMANI |
| REVISED: Feb Sep 2 1978 | PAGE: 1 OF 1 | |



Scalar Processor Design Review Overview

Functionality

- Instruction Processor
- Scalar Processor
- Data Cache
- Return Data Queue

Board Partitioning

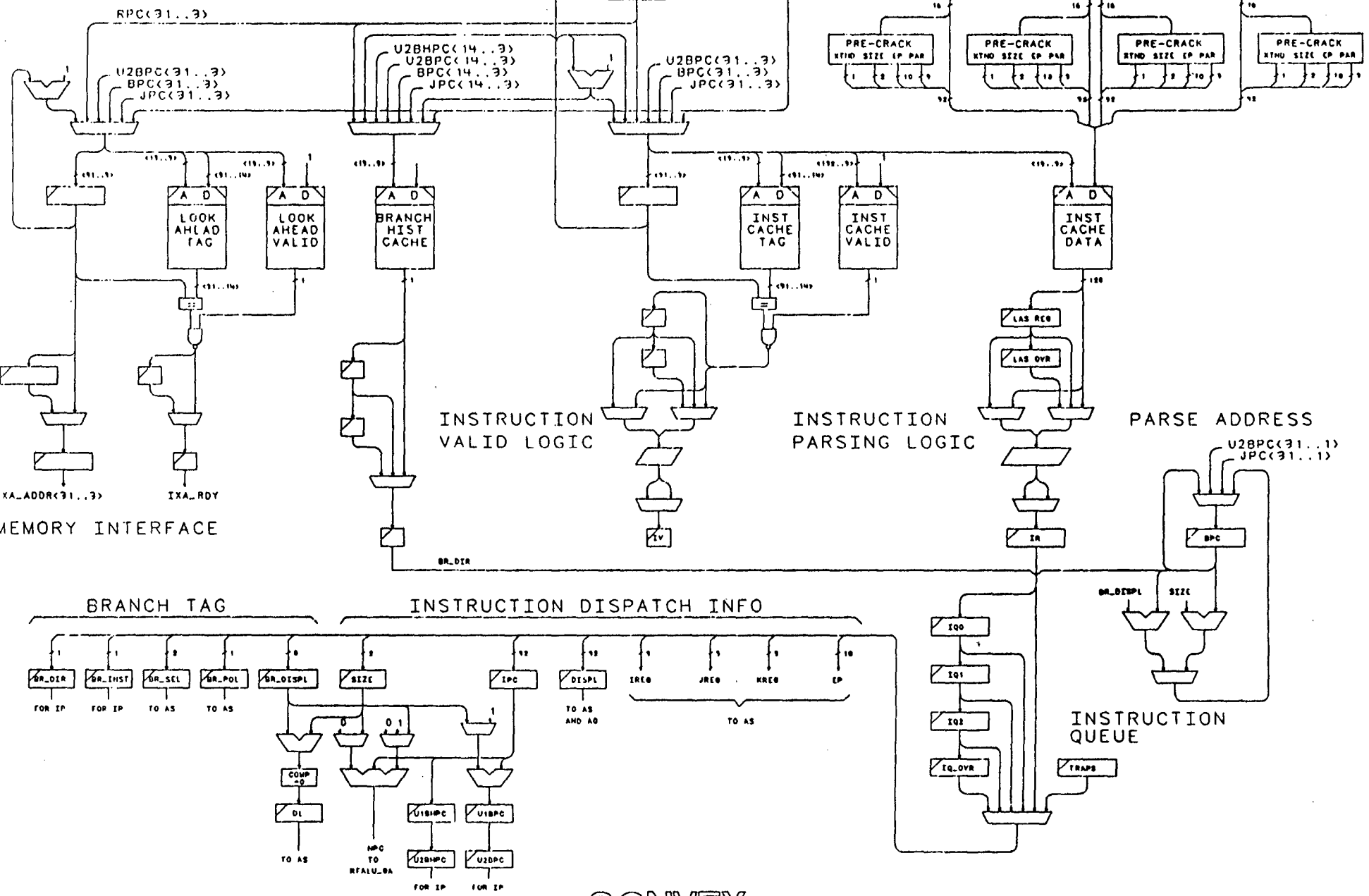
Parts Summary

Testability

Software Impact

NEPTUNE INSTRUCTION PROCESSOR

LOOKAHEAD ADDRESS



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Figure 1

NEPTUNE
BRANCH TAGGING EXAMPLE

INSTRUCTIONS IN MEMORY

```
          SUB.W   S1,S1
STRCMP: LD.B    0(A1),S0
          LD.B    0(A2),S1
          ADD.W   #1,A1
          ADD.W   #1,A2
          EQ.W    S1,S0
          BRS.F   EXITCMP
          EQ.W    #0,S0
          BRS.F   STRCMP
```

EXITCMP:

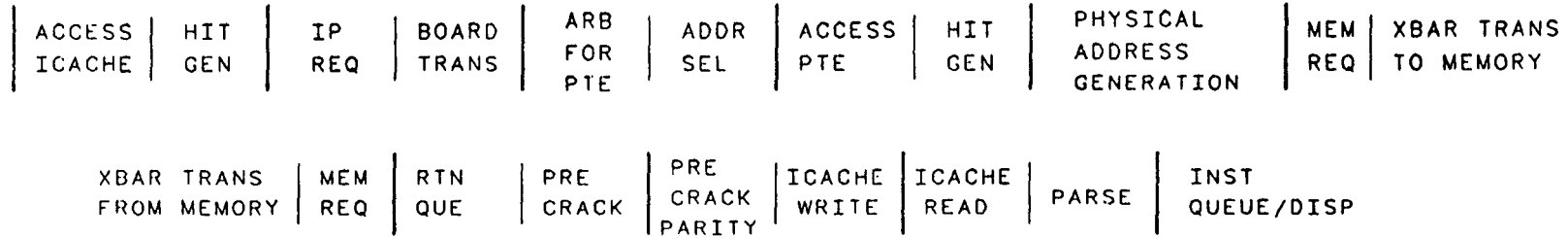
DISPATCHED INSTRUCTIONS

| BRANCH TAG | INSTRUCTION |
|------------|---------------|
| BRS.F | LD.B 0(A1),S0 |
| | LD.B 0(A2),S1 |
| | ADD.W #1,A1 |
| | ADD.W #1,A2 |
| | EQ.W S1,S0 |
| BRS.F | EQ.W #0,S0 |

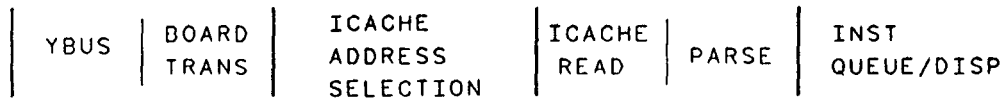
NEPTUNE IP

PERFORMANCE PATHS

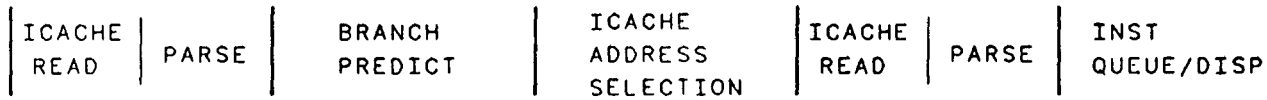
PREFETCH



JUMP/USEQ BRANCH RESTART



BRANCH PREDICT RESTART

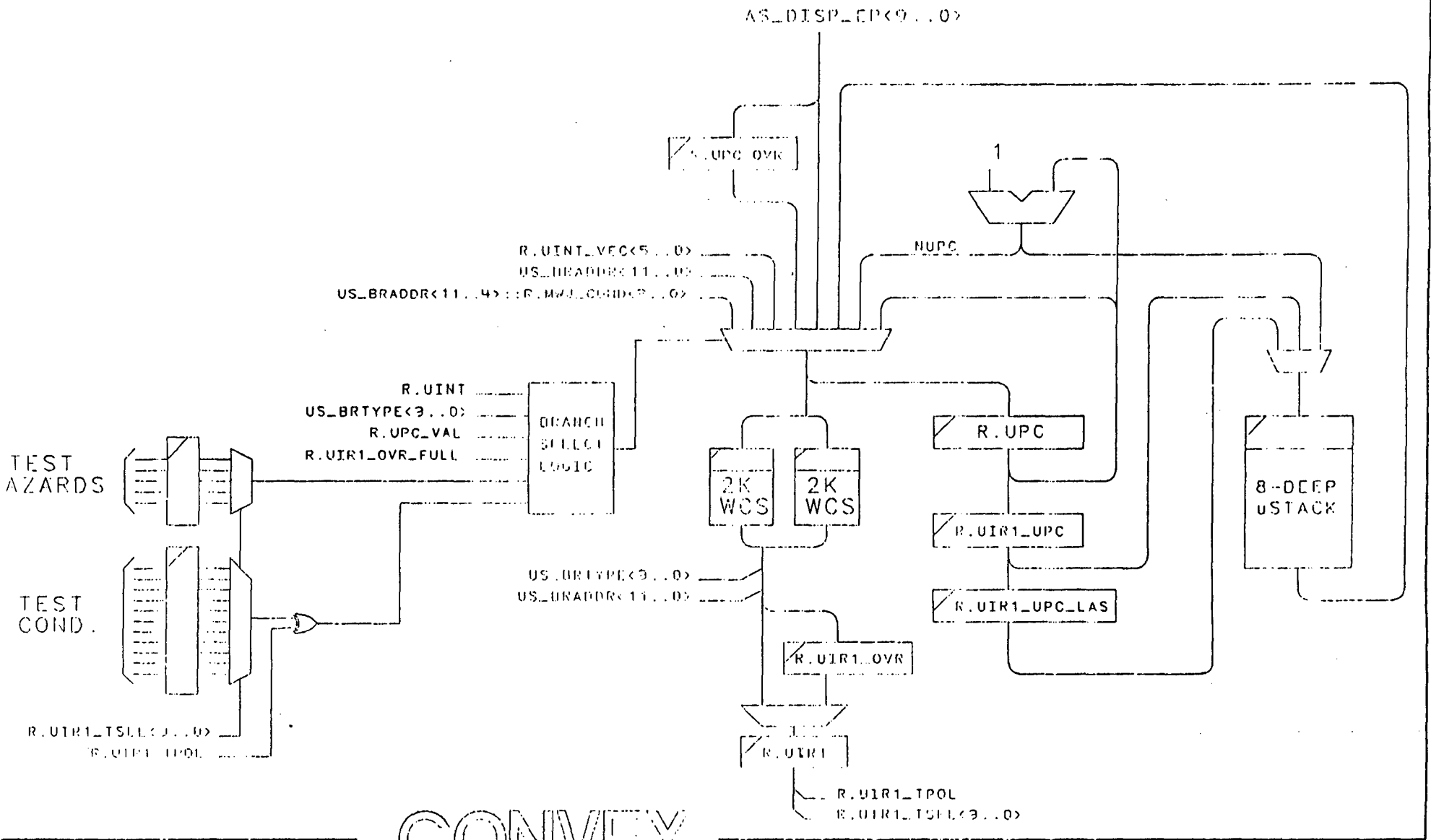


CONVEX

Figure

NEPTUNE

SCALAR PROCESSOR MICROSEQUENCER

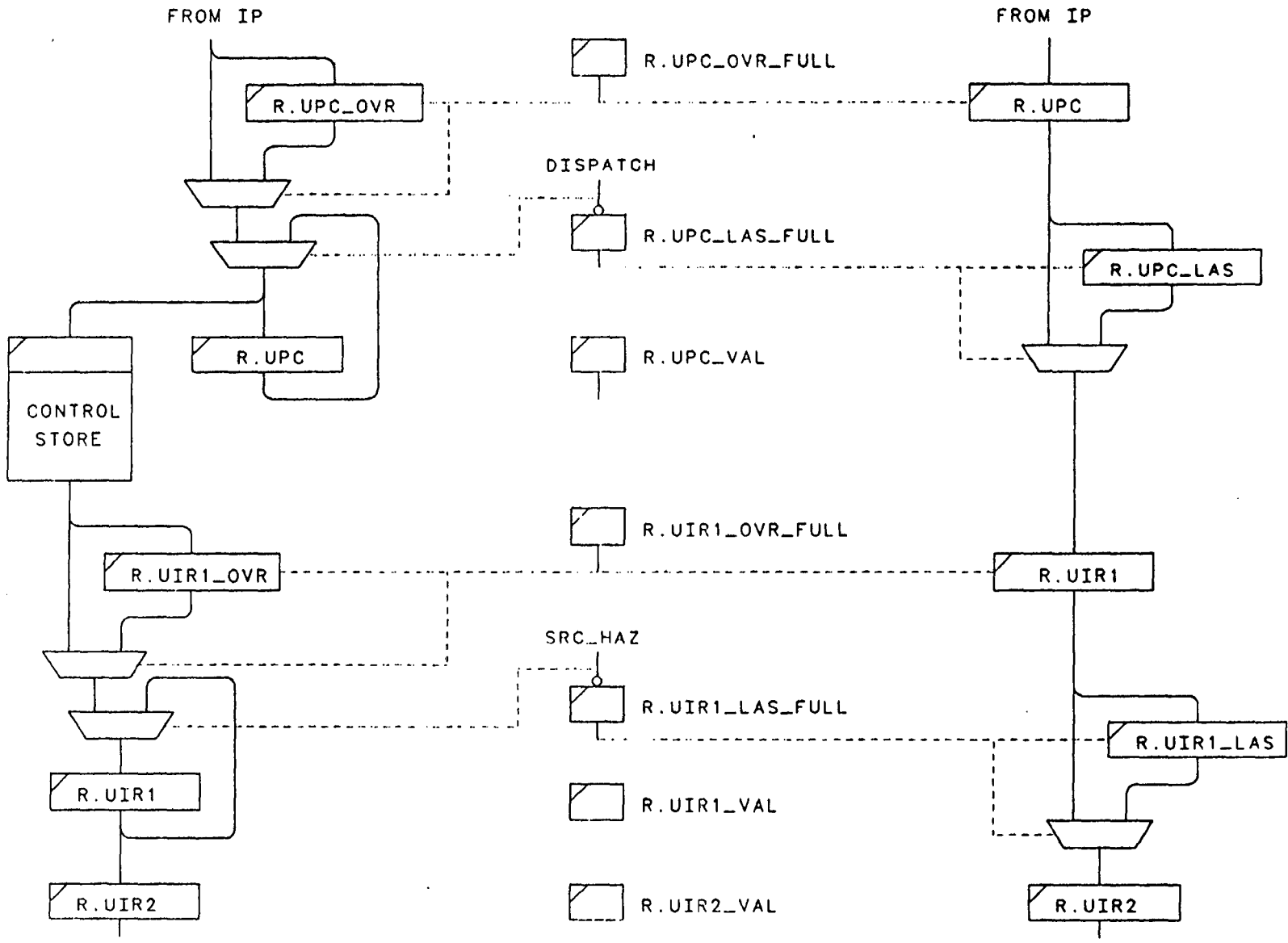


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Figure 4

NEPTUNE USEQ

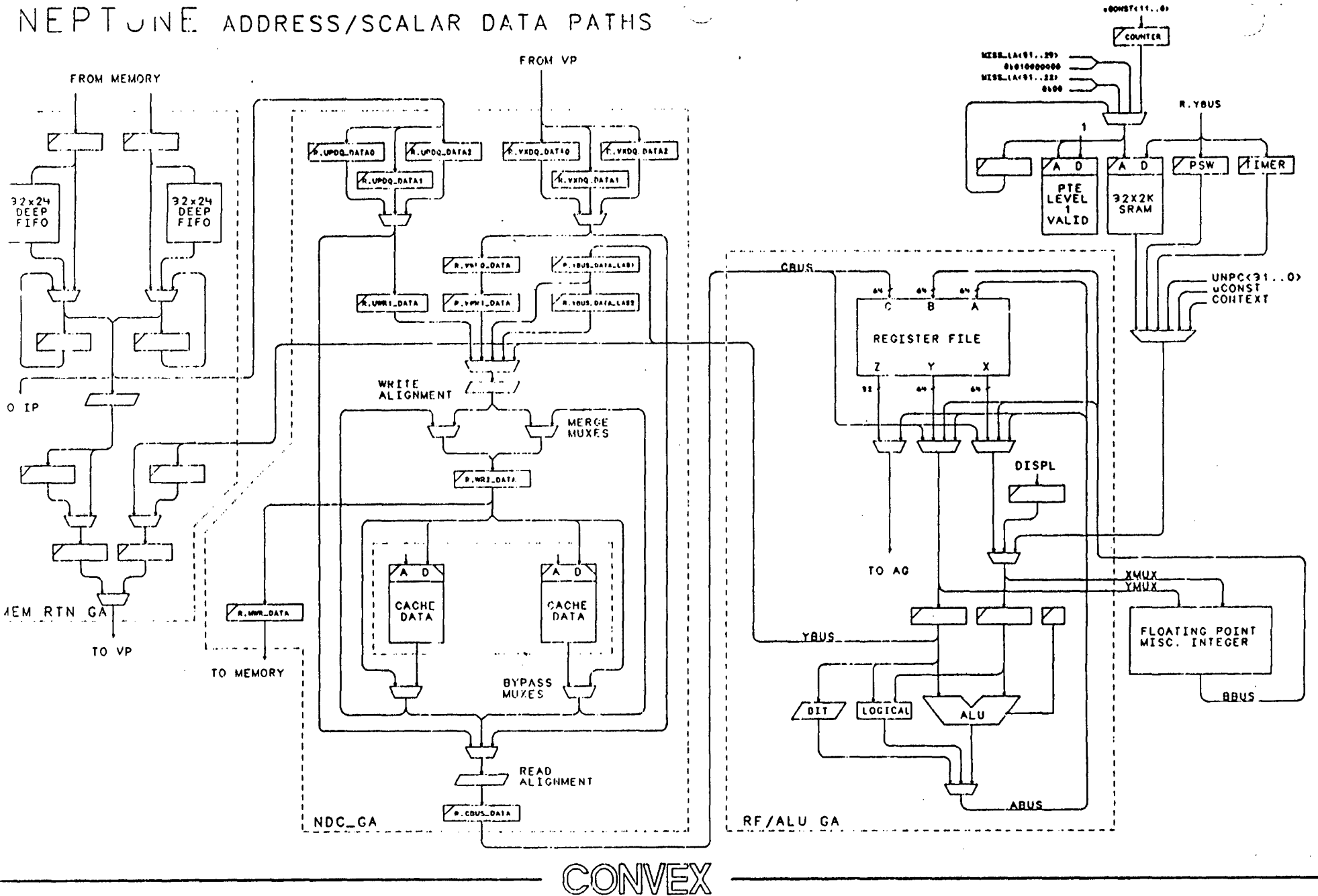
PIPELINE STAGES



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Figure

NEPTUNE ADDRESS/SCALAR DATA PATHS



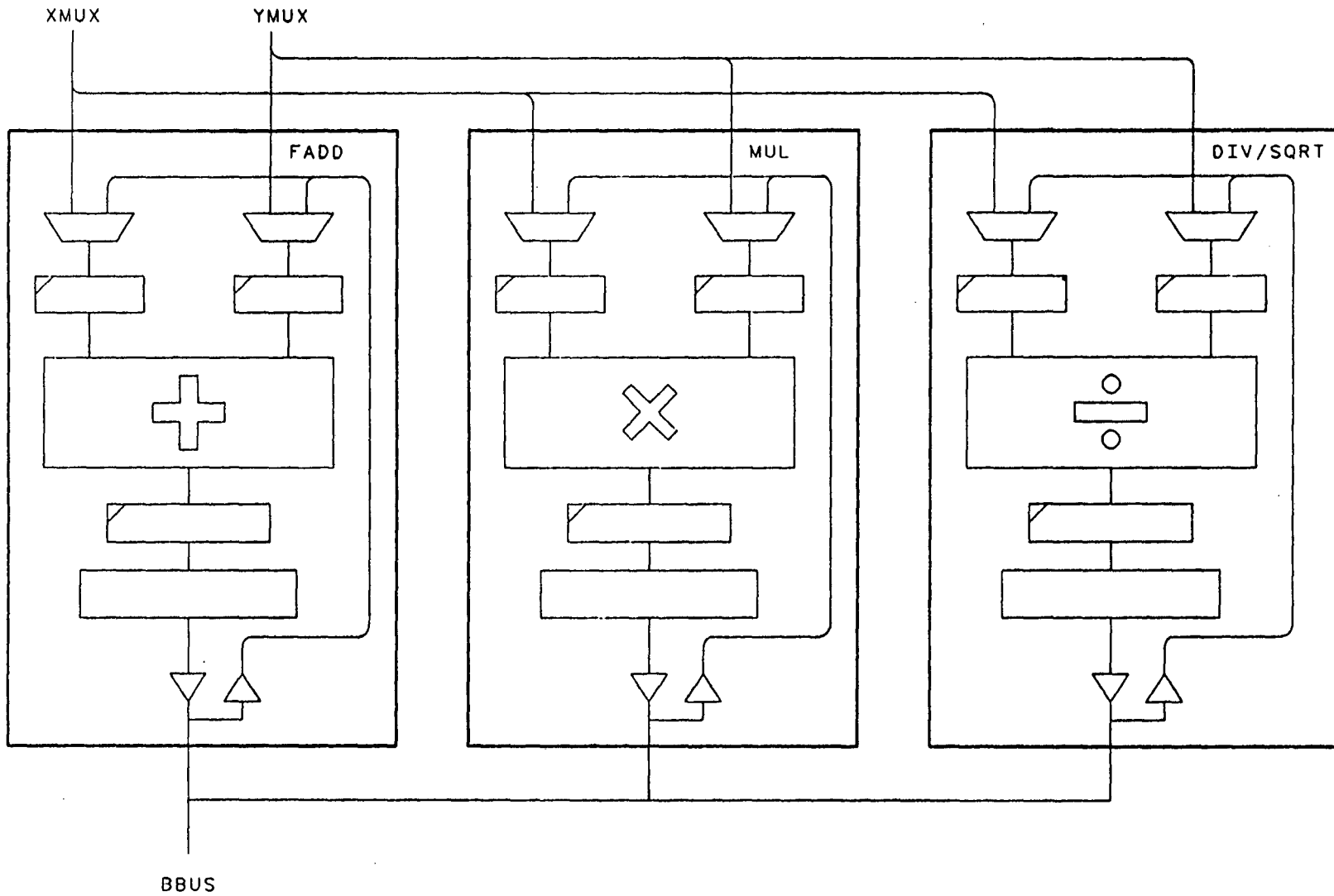
CONVEX

Figure 2

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NEPTUNE

FUNCTION UNITS

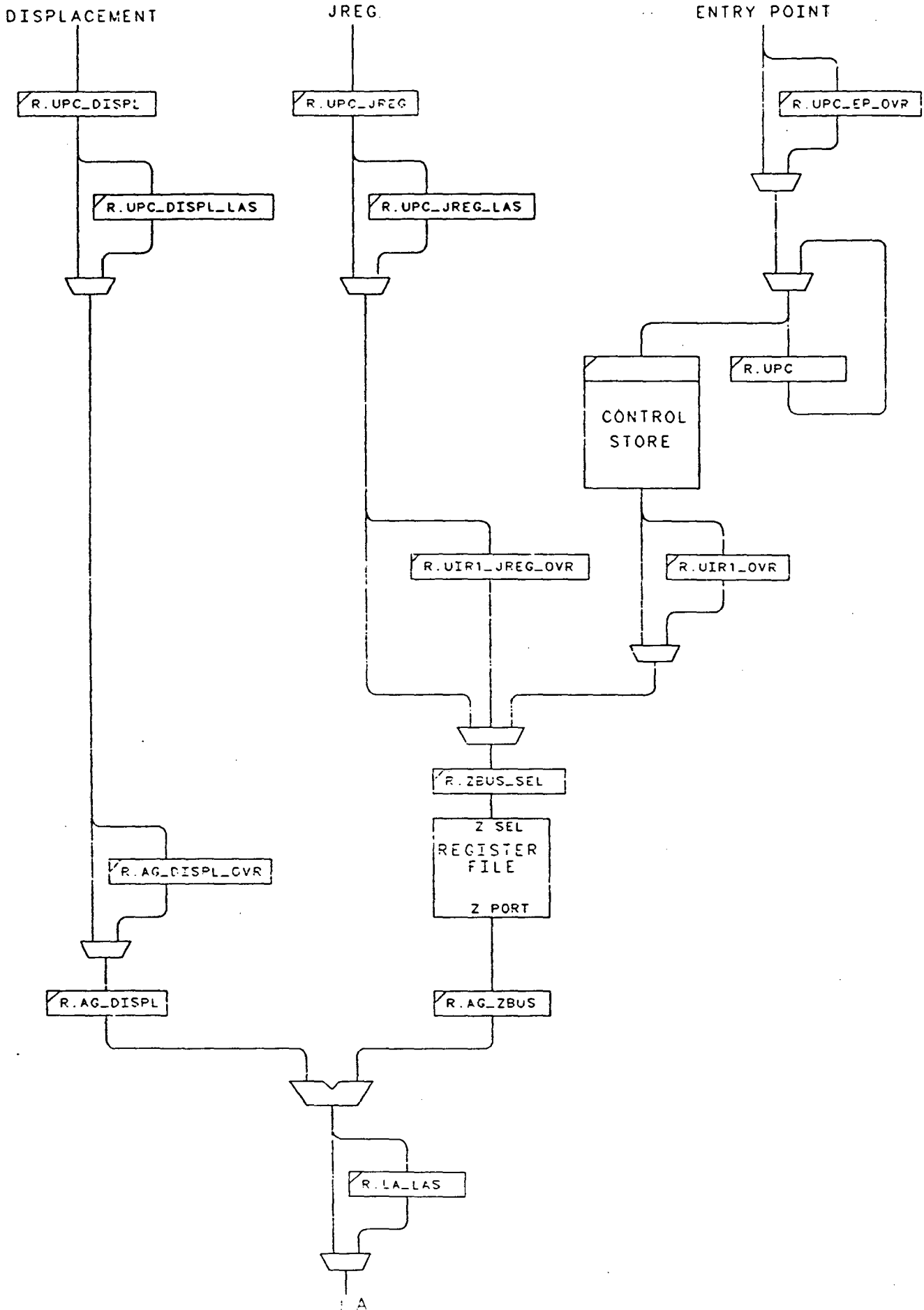


CONVEX

Figure

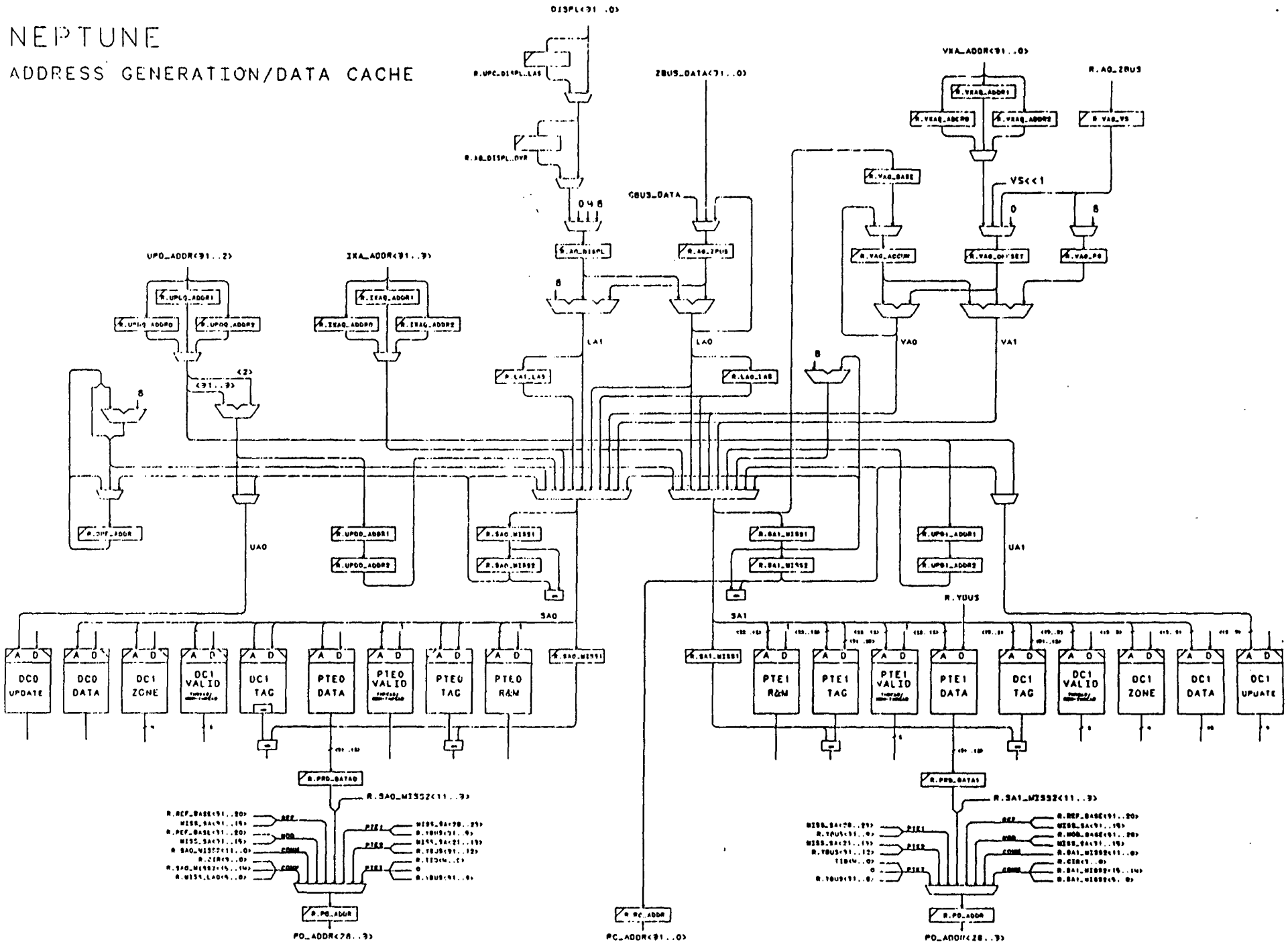
46

NEPTUNE ADVANCED EFFECTIVE ADDRESS



NEPTUNE

ADDRESS GENERATION/DATA CACHE



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Figure 3

NEPTUNE DC

PERFORMANCE PATHS

CACHE READ

| UPC LEVEL | UIR1 LEVEL | | UIR2 LEVEL | | |
|----------------------|------------|-------------|------------------|------------|---------------------------|
| RF READ ZBUS PORT | LA GEN | ADDR SEL | ACCESS PTE/DC | HIT GEN | CBUS WRITE BYPASS READ |

INDIRECT CACHE READ

| UPC LEVEL | UIR1 LEVEL | | UIR2 LEVEL | | | LA | ADDR | ACCESS | HIT | CBUS WRITE |
|----------------------|------------|-------------|------------------|------------|-------------|-----|------|--------|-----|-------------|
| RF READ ZBUS PORT | LA GEN | ADDR SEL | ACCESS PTE/DC | HIT GEN | CBUS BYPASS | GEN | SEL | PTE/DC | GEN | BYPASS READ |

MEMORY READ

| UPC LEVEL | UIR1 LEVEL | | UIR2 LEVEL | | | MEM | XBAR TRANS |
|----------------------|---------------------------|-------------|------------------|-------------|-----------------------------------|-----|------------|
| RF READ ZBUS PORT | LA GEN | ADDR SEL | ACCESS PTE/DC | MISS GEN | PHYSICAL ADDRESS GENERATION | REQ | TO MEMORY |
| | XBAR TRANS FROM MEMORY | MEM RDY | RTN QUE | ROT | CBUS WRITE BYPASS | | |

CACHE WRITE

| UPC LEVEL | UIR1 LEVEL | | UIR2 LEVEL | | | MEM | XBAR TRANS |
|----------------------|------------|-------------|------------------|-------------|------------------------|-----|------------|
| RF READ ZBUS PORT | LA GEN | ADDR SEL | ACCESS PTE/DC | YBUS ROT | ZONE/ DATA MCRGE | REQ | TO MEMORY |
| | | | | | DC WR PA GEN | | |

CONVEX

Figure

NEPTUNE AS

PERFORMANCE PATHS

AS STAGES

| INST DISP | | UPC LEVEL | UIR1 LEVEL | UIR2 LEVEL | |
|----------------|-------------------|------------------------------------|-------------------------------|------------|-----------------|
| BOARD TRANS | CS ADDR SEL | CONTROL STORE ACCESS/ FANOUT | BR/HAZ CHECKS RF RD/BYPASS | ALU OP | RF/PSW WRITE |

LD-LD-ADD-ST OPERATION

| | | | | | | | |
|------------|-----|-----|-----|-----|-----|-----|----|
| UPC LEVEL | LD1 | LD2 | ADD | ST | | | |
| UIR1 LEVEL | | LD1 | LD2 | ADD | ADD | ST | |
| UIR2 LEVEL | | | LD1 | LD2 | | ADD | ST |

CONVEX

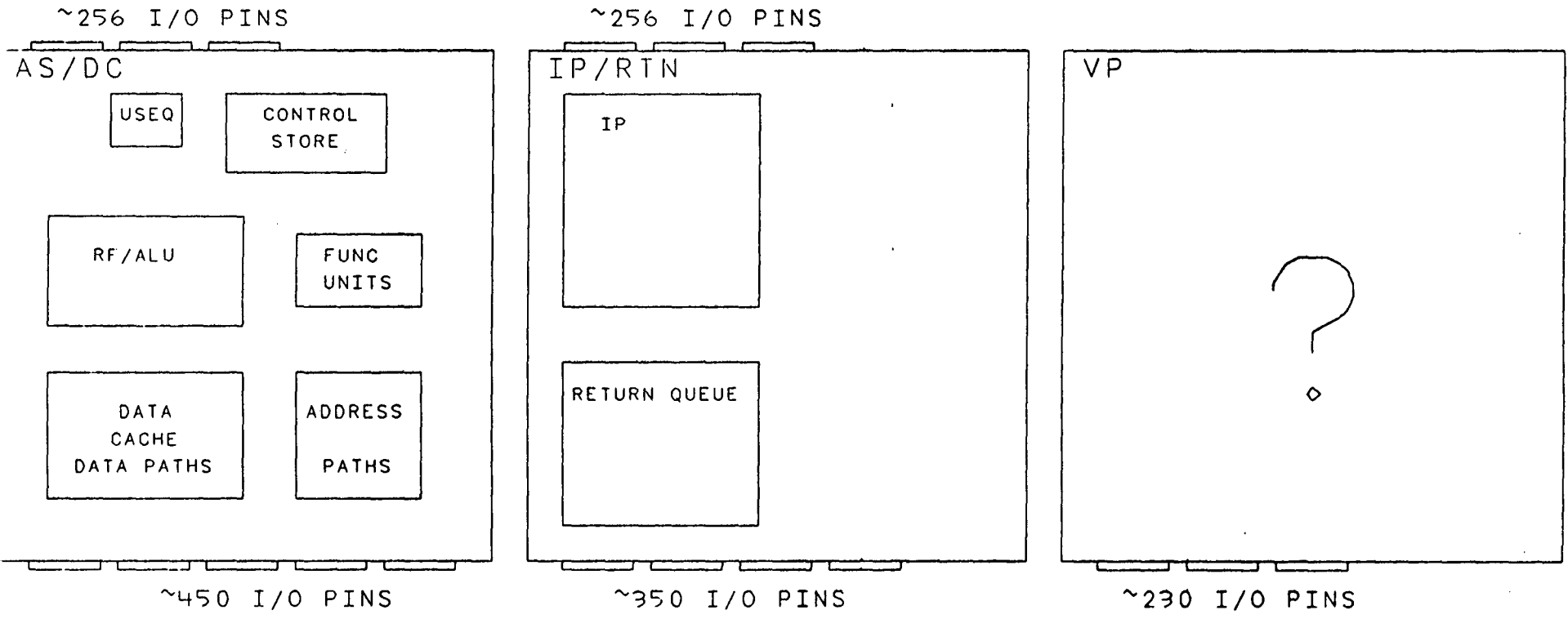
Figure

49

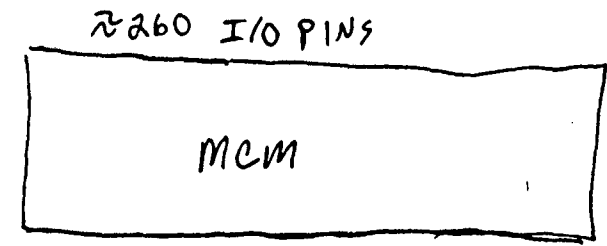
NEPTUNE

BOARD PARTITIONING

FOREPLANE



BACKPLANE



CONVEX

Figure

grr

NEPTUNE PARTS SUMMARY

IP

| | | |
|-------------|----|-------|
| GATE ARRAYS | | |
| ADDRESS | 2 | - 20K |
| INST PARSE | 1 | - 20K |
| STRAM 2KX9 | 21 | |
| STRAM PURGE | 3 | |
| DISCRETE | 55 | |

AS

| | | |
|--------------------|----|-------|
| GATE ARRAYS/CUSTOM | | |
| USEQ | 1 | - 20K |
| RF/ALU | 4 | - 20K |
| FADD | 1 | |
| MUL | 1 | |
| DIV/SQRT | 1 | |
| STRAM 2KX9 | 40 | |
| STRAM PURGE | 1 | |
| DISCRETE | 50 | |

DC

| | | |
|-------------|----|-------|
| GATE ARRAYS | | |
| NDP | 5 | - 10K |
| NAG | 2 | - 20K |
| NPA | 2 | - 20K |
| NDC | 1 | - 10K |
| STRAM 2KX9 | 30 | |
| STRAM PURGE | 12 | |
| DISCRETE | 40 | |

RTNCTL

| | | |
|---------------|----|-------|
| GATE ARRAYS | | |
| DATA QUEUE | 2 | - 20K |
| CONTROL QUEUE | 2 | - 10K |
| DISCRETE | 25 | |

TOTAL

| | | |
|-------------|-----|--|
| GATE ARRAYS | | |
| 10K | 8 | |
| 20K | 14 | |
| CUSTOM | 3 | |
| STRAM 2KX9 | 91 | |
| STRAM PURGE | 16 | |
| DISCRETE | 170 | |

Testability

Parity for Data and Address Paths

- Both internal and between board buses
- This assumes function units will have parity

Self Timed Rams check input parity

- Helps isolate problem quickly

Using Registers for Register File and Queues

- Allows scan based access for CAST and diagnostics

Software Impact

Referenced and Modified Bits

- Main memory based
- Two new instructions: PREF and PMOD

PTE Cache Consistency

- Logically tagged with address and CIR
- Two copies of validity - thread and non-thread
- Compatible with C2

Data Cache Consistency

- Logically tagged with address and CIR
- Two copies of validity - thread and non-thread
- Compatible with C2

Degraded Data Cache Size for OS use

- Cache size under control of micro code
- Micro code will degrade cache for inward ring calls (sysc)
- Micro code will purge entire cache for outward returns
- Compatible with C2